In the Specification:

Please replace the paragraph starting on line 16 of page 6 and ending on line 26 of page 6 with the following paragraph:

In accordance with one example embodiment, the non-destructive FIFO is used as a cache to enable a loop of instructions to be executed a desired number of times. An advantage of the FIFO of the present invention over typical cache memory devices that are used for this purpose is that cache memory requires that ~~the~~ a check be performed to determine if the correct data is in the cache before it is read from the cache. In contrast, if the FIFO of the present invention is used for multiple executions of a loop of instructions, it is known that the data is in the FIFO, and therefore there is no need to check to determine if the correct data is in the FIFO. The loop can be executed multiple times by simply resetting the read pointer to the address of the FIFO containing the first instruction of the loop after the read pointer has been incremented to the address containing the last instruction of the loop.

Please replace the three paragraphs starting on page 6, line 14 and ending on page 7, line 17 with the following paragraph:

Fig. 5 illustrates the method of the present invention in accordance with the example embodiment of Fig. 4. This example assumes a loop that is to be executed 10 times that comprises 8 instructions. The empty flag is set since this is the first time the loop of instructions has been stored in the FIFO. The write address pointer begins at the first location in the FIFO and stores the first instruction at that location, as indicated by block 41. The write address counter is incremented each time a value is stored in the FIFO, as indicated by block 42. A determination is then made as to whether the write address counter has been incremented to 8, as indicated by decision block 43. If not, the process moves to block 44 and the next value is stored at the next address in the FIFO. The process then returns to decision block 43 and if the write address counter has not yet been incremented to 8, moves again to block 44 and the next value is stored at the next address.

Once the write address counter has been incremented to 8, the full flag is set, as indicated by block 46. When the read signal is asserted, the read address pointer will cause the value stored at the first location in the FIFO to be read out of the FIFO, as indicated by block 47. The read address counter will then be incremented, as indicated by block 48. A determination will then be made as to whether the read address counter is equal to 8 or greater than the current write address, as indicated by block 49. If neither of these conditions is true, the process will proceed to block 51 and the next value stored at the location of the read address pointer will be read out of the FIFO. Each time a value has been read from a location in the FIFO identified by the read address, ~~as indicated by block 52. A~~a determination will then be made as to whether the read address counter has been incremented to 8 OR whether it is greater than the write address, as indicated by block 49~~53~~. If neither of these conditions are true, the read address counter will be incremented to the next address and the value stored at the address identified by the read address pointer will be read out of the FIFO, as indicated by block 51~~54~~. The process will continue to return to decision block 49~~53~~ and then on to block 51~~54~~ until either of the conditions identified in block 49~~53~~ is satisfied. ~~Once this happens, the empty flag will be set, as indicated by block 55.~~

A determination is then made as to whether the 10 passes through the loop have been made. This can be accomplished in a number of ways, such as by incrementing a counter when the empty flag has been set, as indicated by block 52~~6~~, and then determining whether the counter equals 10, as indicated by block 53~~7~~. If a determination is made that 10 passes have not been made, ~~the read address counter is reset, as indicated by block 58. T~~the process then returns to block 47~~1~~ and proceeds again through the aforementioned steps. If a determination is made at block 53~~7~~ that 10 passes have been made, then the write address and read address counters are cleared, as indicated by block 54~~9~~.